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ART UNIT: 2816

FROM: Winston Hsu, PATENT AGENT, REG. NO.: 41,526

**SERIAL NO.: 09/682,303** 

ATTORNEY DOCKET NO.: NAUP0303USA

SUBJECT: INFORMATION DISCLOSURE STATEMENT

**TOTAL PAGES: 22 PAGES (INCLUDING COVER PAGE)** 

Winston Hsu 2004/10/21

PTC/SE/97 (09-04)

Approved for use through 07/31/2008, OMB 0651-0031

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				Art Unit	2816		
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Effective 10/01/2004. Patent fees are subject to annual revision	_	First	Named	Inver	ntor Jui-Lu	Lung Chen		
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## PATENT

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Jui-Lung Chen Shih-Huang Huang

5 Examiner: An T. Luu

Filing Date: 08/16/2001 Art Unit: 2816

App. No.: 09/682,303 Docket No.: NAUP0303USA

Title: DELAY LOCK CIRCUIT USING BISECTION ALGORITHM AND

10 RELATED METHOD

To: Commissioner of Patents

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Subject: Information disclosure statement Under

37C.F.R.\$1.56 and 37C.F.R.\$1.97(d).

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Dear Sir or Madame:

This is an Information Disclosure Statement in accordance with the duty to disclose information material to patentability under 37 C.F.R. \$1.56. Applicants wish to make of record the document listed on the accompanying form PTO/SB/08. It is respectfully requested that the Examiner initial the cited references on the form and that it be made of record in the application and that a copy of the initialed form be sent to Applicants with the next communication from the Examiner.

Since the IDS is filed after the mailing date of a notice of allowance, and on or before a payment of the issue fee, the requirement set forth in \$1.97(d) is satisfied. Items of information contained in the information disclosure statement were cited in communication from PRC Patent Office on 07/25/2004 for a counterpart foreign application.

The cited reference, JP publication number No. H10-13219, teaches a DLL circuit. As shown in Fig.1, the block diagram discloses a configuration of the cited art DLL circuit 14. The DLL circuit 14 comprises a phase detector 11 for comparing the phase difference between the external clock signal 6 and the internal clock signal 7, a control signal generating circuit 13 for generating a control signal according to the comparison results 8-1, 8-2, 9-1, 9-2, and 15 10 of the phase detector 11, a plurality of delay units 3 for delaying the external clock signal 6, a multiplexer 4 for selecting a certain number of the delay units 3 according to the control signal outputted from the control signal generating circuit 13, and a clock driver 5 for generating 20 the internal clock signal 7 according to the selected delay . units. A delay unit 3 is a smallest unit, which delays the external clock signal 6. Since the control signal generating circuit 13 is capable of determining a total number of used 25 delay unit 3 according to a comparison result generated from the phase detector 11, it transmits the control signal to the multiplexer 4 for driving the multiplexer 4 to select the required delay units 3.

Independent Claim 11 of the present invention, listed in the response to the Office action dated 06/03/2004, is repeated here for reference.

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- 11. A delay lock circuit for generating a second clock according to a first clock and synchronizing the first clock and the second clock, the delay lock circuit comprising:
  - a comparator for determining if corresponding periods of the first clock and the second clock are synchronized and generating a corresponding comparison signal;
  - a delayer electrically connected to the comparator for delaying the first clock so as to change a delay time between the corresponding periods of the first clock and the second clock; and

a controller to control the delay lock circuit; wherein the controller uses the delayer to perform a correcting process to increase or decrease the delay time between the corresponding periods of the first clock and the second clock by a correction interval, wherein a subsequent correction interval of a subsequent correcting process is less than a previous correction interval of a previous correcting process, and the controller terminates the correcting process if the correction interval is smaller than a predetermined value.

that "a subsequent correction interval of a subsequent correcting process is less than a previous correction interval of a previous correction interval of a previous correcting process." Based on the above difference, it is believed that claim 11 is substantially different from the cited reference. And claims 12-14 are dependent on claim 11, they are believed to be substantially different from the cited reference.

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Independent Claim 16 of the present invention, listed in the response to the Office action dated 06/03/2004, is repeated here for reference.

5 16. A method for performing a delay lock to generate a second clock according to a first clock and to synchronize the second clock with the first clock, the method comprising: executing a plurality of correcting processes, each of which increases or decreases by a respective correction interval a respective delay time between corresponding periods of the first clock and the second clock; and

terminating the plurality of correcting processes when the correction interval is smaller than a predetermined value;

wherein a subsequent correction interval for a subsequent correcting process is less than a previous correction interval of a previous correcting process.

Similarly, as mentioned above, the cited reference fails to teach or suggest that "a subsequent correction interval of a subsequent correcting process is less than a previous correction interval of a previous correcting process." Based on the above difference, it is believed that claim 16 is substantially different from the cited reference. And claims 17-24 are dependent on claim 16, they are believed to be substantially different from the cited reference.

Sincerely yours,

5 Winten Han

Date: October 21, 2004

Winston Hsu, Patent Agent No. 41,526

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U.S.A.

10 Facsimile: 806-498-6673

e-mail: winstonhsu@naipo.com

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Complete if Known Substitute for form 1449/PTO Application Number 09/682,303 Filing Date 08/16/2001 INFORMATION DISCLOSURE First Named Inventor Jui-Lung Chen STATEMENT BY APPLICANT Art Unit 2816 (Use as many sheets as necessary) Examiner Name LUU, AN T Attorney Docket Number NAUP0303USA Sheet 1

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